Brasília, 29 de dezembro de 2005

Sr. Pregoeiro,

Em referência ao pregão 120/2005, vimos prestar as conclusões definitivas da nossa análise encerrada nesta data.

Com relação à proposta da licitante de menor preço, o equipamento ofertado, modelo ND P500-M240Z deixou de atender às especificações técnicas no seguinte quesito:

- *Memória*
- *...*
- *Deverá suportar tecnologia Memory Sparing ou superior, permitindo que falhas em ranks (chips) de memória não afetem o funcionamento normal do sistema operacional.*

Em se tratando de funcionalidade indispensável para garantir os níveis de confiabilidade e alta disponibilidade requeridos pelas aplicações críticas para as quais se destinam os equipamentos pretendidos, consideramos inaceitável a proposta da licitante Novadata Sistemas e Computadores S/A para a licitação em tela.

Efetuado o exame das características técnicas e de suporte de serviços da proposta classificada em segundo lugar no certame, tendo sido ofertado um equipamento de marca IBM, modelo X-Series-346 com os componentes abaixo relacionados, foi verificado que o mesmo atende integralmente aos requisitos do Edital.

Itens de hardware analisados (relacionados na proposta):

8840-D1U-LM (79) - x346 Dual-Core
73P4792 (316) - RAM
90P1381 (158) - HD's
71P8642 (79) - SCSI RAID Adapter
73P4101 (79) - Gigabit Ethernet cobre
24P0960 (158) - HBA's
26K5097 (79) - Fonte adicional
73P9341 (79) – RSA

Assim, posicionamo-nos pela desclassificação da proposta de menor preço e adjudicação do certame para a segunda proposta de menor preço, considerando, ainda, ser valor unitário cotado nesta última ligeiramente superior ao da primeira.

Para constar, encaminho informações pesquisadas a respeito do item em desconformidade que ensejou a proposta de desclassificação (informações em inglês). Esclareço que nível de redundância e alta disponibilidade exigido para os *chips* de memória e proporcionado pela tecnologia de "memory sparing" conforma-se com o exigido para os demais componentes como processador, controladora "RAID", discos, placas de rede, adaptadores "fiber-channel" e fontes de alimentação:

Memory Spares: Allows a failed memory device to be transparently replaced by a spare device. This improves performance, by eliminating the performance loss caused by ECC correction. It also improves reliability, since it can correct multiple soft errors in a memory device (ECC can only correct single errors). Enables correction of multiple DRAM devices.

Online Spare Memory - Online Spare Memory uses an online spare bank to provide DIMM failover capabilities when a pre-defined threshold of single-bit correctable errors is reached. (see figure below)

Chipkill - Memory Single Device Error Correction (SDEC) or chipkill: Enables the system to correct all memory errors if a single DRAM device fails.

Traditional ECC memory can only detect and correct single bit errors and can only detect two bit errors. Single bit errors are the most common type of memory error. ECC can correct about 90% of all memory errors.

Chipkill (developed by IBM) is the ability for the memory subsystem to detect and correct multibit errors in memory. This is done by writing a checksum to another part of the memory subsystem and then recalculating the correct data. These are 2, 3, and 4 bit errors, and in some cases this can even cover an entire DRAM chip. Chipkill can supposedly correct about 99% of all memory errors.

This small paper gives a basic summary of chipkill: http://www-5.ibm.com/hu/termekismertetok/xseries/dn/chipkill.pdf and a much more detailed paper is available here:

http://www-03.ibm.com/servers/eserver/pseries/campaigns/chipkill.pdf

Memory sparing is basically a method for the system to swap in a spare DIMM when another DIMM has exceeded some threshold of correctable errors. For example, DIMM 1 is actively used by the system while DIMM 2 is unused and in reserve. The system monitors the number of ECC errors that occur on DIMM 1 and after too many have occurred, it copies all the contents of DIMM 1 to DIMM 2 and then turns off DIMM 1, marks it as bad, and then only uses DIMM 2. This allows the system to continue operating until the system administrators can service the server and replace the faulty memory.

Section 10.1.1 of the Harwich product spec covers this process:
ftp://download.intel.com/support/motherboards/server/sb/se8500hw4_board_set_tpsr10.pdf

Memory sparing and chipkill are not exclusive technologies. Sun's UltraSPARC and some other servers I believe use both types of memory reliability schemes.

In conjunction with Chipkill, DRAM sparing is implemented in the UltraSPARC T1 processor to improve main memory availability. Where Chipkill detects a failed DRAM chip, DRAM

sparing reconfigures a DRAM channel to map out the failed chip, effectively replacing it with a corrected DRAM chip. This technique restores the capability of correcting any random single-nibble error and allows the system to run with minor impaired memory error protection until the DIMM can be replaced.

http://www.intel.com/business/bss/products/server/ras.pdf.

"Xeon processors with 64-bit extensions and Itanium processors are both engineered with on-chip reliability and scalability enablers, including memory spares, chipkill memory, and error correction codes (ECC). "

http://www.intel.com/technology/64bitextensions/idc_intel_xeon_whitepaper.pdf

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Atenciosamente

ORIGINAL ASSINADO

Jorge Lobo
SRPP/Seprod